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EXAMINER	
CHEN, XIAOLIANG	
ART UNIT	**PAPER NUMBER**
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,796	AMBO ET AL.	
	Examiner	Art Unit	
	XIAOLIANG CHEN	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2006* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08-02-07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-10 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers et al. (US5456608) in view of Nakayama (US5434749).

Re Claim 1, Regers show and disclose

A circuit board (10, fig. 2) comprising

a three-dimensional plate (circuit board 10, fig. 3), and a circuit pattern (trace 21, fig. 3) of metal foil placed on said plate;

Rogers et al. does not disclose

the plate being an insulating synthetic resin plate,

Nakayama teaches a device wherein

the plate being an insulating synthetic resin plate (the printed circuit board comprises an insulating substrate of synthetic resin [Abstract]),

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the insulating synthetic resin circuit board as taught by Nakayama in the electronic device of Rogers et al., since the printed circuit board made of insulating synthetic resin is well known and most common in the art at the time the invention was made, and it is inexpensive.

Re Claim 2, Regers show and disclose

The circuit board according to claim 1, wherein said circuit pattern is formed by at least one foil circuit punched out of a metal foil into a given pattern, (Examiner's notes: with respect to "is formed by", which is a process limitation. The process limitation does not carry weight in a claim drawn to structure or device. When the reference teaches a product that appears to be the same as, or an obvious variant of, the product set forth in a product-by-process claim although produced by a different process. See In re Marosi, 710 F.2d 799, 218 USPQ 289 (Fed. Cir. 1983) and In re Thorpe, 777 F.2d 695, 227 USPQ 964 (Fed. Cir. 1985). See MPEP § 2113.), said foil circuit being fixed onto said resin plate (fig. 3).

Re Claim 3, Regers show and disclose

The circuit board according to claim 2, wherein said circuit pattern includes a plurality of pin receiving holes (20, fig. 3) into which anchor pins (connecting pin 40, fig. 4) extending from the resin plate are inserted to fix said circuit pattern onto the resin plate (fig. 7).

Re Claim 4, Regers show and disclose

The circuit board according claim 1, wherein said resin plate has at least one recess (recess for holding 102, fig. 7) formed in a rear surface (bottom, fig. 7) thereof, and both ends (102, fig. 7) of a jumper wire (101, fig. 7) held in said recess are connected to said circuit pattern (fig. 7).

Re Claim 5, Regers show and disclose

The circuit board according to claim 2, wherein said circuit pattern is formed by a plurality of metal foils (21-28, fig. 3) which are stacked on said resin plate.

Re Claim 6, Regers show and disclose

A circuit board (10, fig. 2) comprising

a three-dimensional plate (circuit board 10, fig. 3), and a circuit pattern (trace 21, fig. 3) of metal foil placed on said plate, and a plurality of reception terminals (female contacts 30, fig. 3) provided in a plurality of terminal receiving holes (20. fig. 3) formed in said plate such that said reception terminals are connected to said circuit pattern (fig. 3).

Rogers et al. does not disclose

the plate being an insulating synthetic resin plate,

Nakayama teaches a device wherein

the plate being an insulating synthetic resin plate (the printed circuit board comprises an insulating substrate of synthetic resin [Abstract]),

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the insulating synthetic resin circuit board as taught by Nakayama in the electronic device of Rogers et al., since the printed circuit board made of insulating synthetic resin is well known and most common in the art at the time the invention was made, and it is inexpensive.

Re Claim 7, Regers show and disclose

The circuit board according to claim 6, wherein said reception terminal includes a tab portion (the portion extents from contact 30 and connecting the circuit pattern together, fig. 3) connect to said circuit pattern. (Examiner's notes: with respect to "is welded", which is a process limitation. The process limitation does not carry weight in a claim drawn to structure or device. When the reference teaches a product that appears to be the same as, or an obvious variant of, the product set forth in a product-by-process claim although produced by a different process. See In re Marosi, 710 F.2d 799, 218 USPQ 289 (Fed. Cir. 1983) and In re Thorpe, 777 F.2d 695, 227 USPQ 964 (Fed. Cir. 1985). See MPEP § 2113.)

Re Claim 8, Regers show and disclose

A circuit board (10, fig. 2) comprising

a three-dimensional plate (circuit board 10, fig. 3), and a circuit pattern (trace 21, fig. 3) of metal foil placed on said plate, and a plurality of tubular

reception terminals (female contacts 30, fig. 3) clamped in a plurality of terminal receiving holes (20. fig. 3) formed in said plate (fig. 3); whereby said metal foil of the circuit pattern has formed therein a plurality of cut portions (cut portions for the receiving holes, fig. 3) at positions corresponding to said terminal receiving holes such that a plurality of connection terminals (connecting pin 40, fig. 4) can be inserted into said reception terminals through said cut portions (fig. 7).

Rogers et al. does not disclose

the plate being an insulating synthetic resin plate,

Nakayama teaches a device wherein

the plate being an insulating synthetic resin plate (the printed circuit board comprises an insulating substrate of synthetic resin [Abstract]),

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the insulating synthetic resin circuit board as taught by Nakayama in the electronic device of Rogers et al., since the printed circuit board made of insulating synthetic resin is well known and most common in the art at the time the invention was made, and it is inexpensive.

Re Claim 9, Regers show and disclose

The circuit board according to claim 8, wherein inserting ends of said connection terminals (inserting ends of connecting pin 40, fig. 3) are inserted into said reception terminals through said cut portions formed in said metal foil to electrically connect said metal foil to said insertion terminals (fig. 7).

Re Claim 10, Regers show and disclose

The circuit board according to claim 8 or 9, except for said cut portions are formed as a cross-wire cut; in the instant application, the trace is cut then welded together with the inserting receiving hole (a via), and Regers teaches a via disposed in contact with the traces [col. 2, line 63], they are having similar structure and performing the same function. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to dispose the via in contact with the traces since the examiner takes Official Notice of the equivalence of the via integrated contacting with the traces and the traces cut then welded with the via for their use in the connecting the via with the traces, and the selection of any of these are known equivalents within the level of ordinary skill in the art.

Re Claim 15, Regers show and disclose

A joint box comprising:

a stack of circuit boards (10, fig. 3) each of which is a three-dimensional electrically insulating plate and a circuit pattern (traces 21-28, fig. 3) placed on said insulating plate;

a plurality of terminal receiving holes (20. fig. 3) commonly formed in the stacked circuit boards;

a plurality of tubular metal reception terminals (female contacts 30, fig. 3) each of which includes a tab portion (the portion extents from contact 30 and connecting the circuit pattern together, fig. 3) and is provided in a terminal receiving hole (20. fig. 3) formed in a given layer circuit board of said stack (fig.

3), said tab portion being connected to a circuit pattern of the relevant circuit board (fig. 3); and

a plurality of insertion terminals including pin-shaped inserting ends (connecting pin 40, fig. 4) inserted into said terminal receiving holes such that the insertion terminals are connected to said reception terminals to establish electrically connection between said circuit patterns of the circuit boards (fig. 7). Rogers et al. does not disclose

the insulating plate being an insulating synthetic resin plate,

Nakayama teaches a device wherein

the insulating plate being an insulating synthetic resin plate (the printed circuit board comprises an insulating substrate of synthetic resin [Abstract]),

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the insulating synthetic resin circuit board as taught by Nakayama in the electronic device of Rogers et al., since the printed circuit board made of insulating synthetic resin is well known and most common in the art at the time the invention was made, and it is inexpensive.

Re Claim 16, Regers show and disclose

The joint box according to claim 15, wherein said tab portions of the reception terminals are connected to said circuit patterns (fig. 3) by welding. (Examiner's notes: with respect to "is formed by", which is a process limitation. The process limitation does not carry weight in a claim drawn to structure or device. When the reference teaches a product that appears to be the same as, or

an obvious variant of, the product set forth in a product-by-process claim although produced by a different process. See In re Marosi, 710 F.2d 799, 218 USPQ 289 (Fed. Cir. 1983) and In re Thorpe, 777 F.2d 695, 227 USPQ 964 (Fed. Cir. 1985). See MPEP § 2113.)

Re Claim 17, Regers show and disclose

A joint box comprising:

a stack of circuit boards (10, fig. 3) each of which includes a three-dimensional electrically insulating plate and a circuit pattern (21, fig. 3) placed on said plate;

a plurality of terminal receiving holes (20. fig. 3) commonly formed in the plates of the stacked circuit boards (fig. 3);

a plurality of cut portions (cut portions for the hole 20, fig. 3) formed in said circuit patterns;

a plurality of tubular metal reception terminals (female contacts 30, fig. 3) provided in said terminal receiving holes formed in given layer circuit boards (fig. 3); and

a plurality of insertion terminals having pin-shaped inserting ends (connecting pin 40, fig. 4) inserted into said terminal receiving holes through said cut portions such that the insertion terminals are connected to said reception terminals to establish electrically connection between said circuit patterns of the circuit boards (fig. 7).

Rogers et al. does not disclose

the plate being an insulating synthetic resin plate,

Nakayama teaches a device wherein

the plate being an insulating synthetic resin plate (the printed circuit board comprises an insulating substrate of synthetic resin [Abstract]),

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the insulating synthetic resin circuit board as taught by Nakayama in the electronic device of Rogers et al., since the printed circuit board made of insulating synthetic resin is well known and most common in the art at the time the invention was made, and it is inexpensive.

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers et al. in view of Nakayama and Ishii (US4937932).

Re Claim 11, Regers show and disclose

A method of manufacturing a circuit board (10, fig. 2) comprising

fixing a circuit pattern (21, fig. 3) to a three-dimensional mold of an electrically insulating plate (circuit board 10, fig. 3), transporting said circuit pattern onto said insulating plate (traces are typically plated onto the board surface [col. 5, line 7];

Regers does not disclose

1) the insulating plate formed by an electrically insulating synthetic resin and a circuit pattern placed on said resin plate,

2) punching said circuit pattern out of a metal foil into a given pattern by means of Thompson blades; holding said circuit pattern between said Thompson blades;

Nakayama teaches a device wherein

1) the insulating plate formed by an electrically insulating synthetic resin, (the printed circuit board comprises an insulating substrate of synthetic resin [Abstract]),

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the insulating synthetic resin circuit board as taught by Nakayama in the electronic device of Rogers et al., since the printed circuit board made of insulating synthetic resin is well known and most common in the art at the time the invention was made, and it is inexpensive.

Ishii teaches a device wherein

2) punching said circuit pattern out of a metal foil into a given pattern by means of Thompson blades (sheet material is cut off or punched out by a Thompson blade [col. 1, line 59]); holding said circuit pattern between said Thompson blades (when the sheet material cutting or punching by a Thompson blade, it must hold between the Thompson blades);

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the Thompson blade to punch out the circuit pattern as taught by Ishii in the electronic device of Rogers et al., in

order to cut out the outline of the sheet material and holes having certain fixed size. (Ishii, col. 1, line 60])

5. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers et al. in view of Nakayama and Ishii as applied to claim 11 above, further in view of Ogawa et al. (US5836582).

Re Claim 12, Regers, Nakayama and Ishii disclose

The method according to claim 11, said circuit pattern is held between the Thompson blades (see claim 11 above),

Regers, Nakayama and Ishii do not disclose

wherein said circuit pattern is held by air suction nozzles.

Ogawa et al. teaches a device wherein

said circuit pattern is held by air suction nozzles (the sheet holding means having an suction opening [col. 4, line 53], sheet adheres to the sheet feeding means by air suction [col. 3, line 4]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the air suction as taught by Ogawa et al. for holding the circuit pattern between the Thompson blades in making the electronic device of Rogers et al., in order to be able to hold the circuit pattern between the blades for a safer cutting, placing and holding, and easier mounting and dismounting the circuit pattern.

Re Claim 13, Regers, Nakayama and Ishii disclose

The method according to claim 11, wherein said circuit pattern is placed onto said resin plate, and holding between said Thompson blades (see claim 11 above),

Regers, Nakayama and Ishii do not disclose

said circuit pattern is placed by air blowing portions;

Ogawa et al. teaches a device wherein

said circuit pattern is placed by air blowing portions (sheet held by the sheet holding means, an air injection nozzle [col. line 48]);

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the air blowing as taught by Ogawa et al. for holding the circuit pattern between the Thompson blades in making the electronic device of Rogers et al., in order to be able to hold the circuit pattern between the blades for a safer cutting, placing and holding, and easier mounting and dismounting the circuit pattern.

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers et al. in view of Nakayama and Ishii as applied to claim 11 above, further in view of Rosli et al. (US5718057).

Re Claim 14, Regers, Nakayama and Ishii disclose

The method according to claim 11, wherein said circuit pattern is placed onto said resin plate, and holding between said Thompson blades (see claim 11 above),

Regers, Nakayama and Ishii do not disclose

wherein said circuit pattern is placed by a plurality of pin-shaped pushing rods.

Rosli et al. et al. teaches a device wherein

said circuit pattern is placed by a plurality of pin-shaped pushing rods (The sheet is held by a holding element , which can be pressed by a pneumatically movable push rod. This holding element is also controlled and operated by the system control [col. 5, line 31]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the pneumatically movable push rods as taught by Rosli et al. for holding the circuit pattern between the Thompson blades in making the electronic device of Rogers et al., in order to be able to hold the circuit pattern between the blades for a safer cutting, placing and holding, and easier mounting and dismounting the circuit pattern.

7. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers et al. in view of Nakayama as applied to claims 15 and 17 above, further in view of Hayashi et al. (US6995650).

Re Claim 18, Regers and Nakayama disclose

The joint box according to claim 15 or 17,

Regers and Nakayama do not disclose

the circuit boards include protrusions and depressions and are stacked by clamping corresponding protrusions and depressions one another.

Hayashi et al. teaches a device wherein

the circuit boards include protrusions (positioning protrusions 11b, fig. 5) and depressions (positioning holes 23, fig. 5) and are stacked by clamping corresponding protrusions and depressions one another (fig. 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the positioning protrusions and positioning holes as taught by Hayashi et al. in the circuit boards of the electronic device of Rogers et al., in order to properly align the positions of the stacked circuit boards in the electronic device.

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers et al. in view of Nakayama as applied to claims 15 and 17 above, further in view of Miller et al. (US4950170).

Re Claim 19, Regers and Nakayama disclose

The joint box according to claim 15 or 17, wherein one end of said insertion terminal constitutes said pin-shaped inserting end (connecting pin 40, fig. 4),

Regers and Nakayama do not disclose

the other end constitutes a connecting terminal having such a shape that another connection terminal is clamped into said connecting terminal.

Miller et al. teaches a device wherein

the other end constitutes a connecting terminal (socket 16, fig. 20) having such a shape that another connection terminal (pin 15, fig. 2) is clamped into said connecting terminal (fig. 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the pin terminal and sock terminal at opposite ends of the connecting pin as taught by Miller et al. in the circuit boards of the electronic device of Rogers et al., in order to form continuous electrical circuits from one printed circuit board to the next and any number of printed circuit boards may be interconnected in the electronic device.

9. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers et al. in view of Nakayama and Miller et al. as applied to claim 19 above, further in view of Downes (US20030102357).

Re Claim 20, Regers, Nakayama and Miller et al. disclose

The joint box according to claim 19,

Regers, Nakayama and Miller et al. do not disclose

said inserting end has a rectangular cross section.

Downes teaches a device wherein

said inserting end (pin 26-4, fig. 4A) has a rectangular cross section.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the pin a having a rectangular cross section as taught by Downes in the circuit boards of the electronic device of Rogers et al., in order to use the pins in smaller vias in high-density, micro-soldered connection arrangements (e.g., in situations with vias closer together than in the conventional reflow soldering approach) in the electronic device (Downes, [Abstract]).

10. Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers et al. in view of Nakayama and Miller et al. as applied to claim 19 above, further in view of Eck (US4867691).

Re Claims 21-22, Regers, Nakayama and Miller et al. disclose

The joint box according to claim 19,

Regers, Nakayama and Miller et al. do not disclose

said insertion terminals are secured to at least one block body made of electrically insulating synthetic resin by fixing middle portions of the insertion terminals between the inserting ends and connecting ends to fitting holes formed in said block body, and said block body is placed on one surface of the stack of circuit boards to insert simultaneously said inserting ends of the insertion terminals into said terminal receiving holes formed in the circuit boards; a plurality of anchor pins are provided on a bottom surface of said block body and are inserted into pin receiving holes formed in the stack of circuit boards, and the circuit boards in the stack are fixed to one another by fusing end portions of the anchor pings extending from the other surface of the stack of circuit boards.

Eck teaches a device wherein

said insertion terminals are secured to at least one block body (connector housing body of 40, fig. 8) made of electrically insulating synthetic resin (the polyester engineering thermoplastic resin [col. 5, line 32] by fixing middle portions of the insertion terminals between the inserting ends and connecting ends to fitting holes (fitting holes in the body of the connector, fig. 8) formed in said block

body, and said block body is placed on one surface of the stack of circuit boards (circuit boards, fig. 8) to insert simultaneously said inserting ends of the insertion terminals into said terminal receiving holes (receiving holes for inserting pins, fig. 8) formed in the circuit boards; a plurality of anchor pins (72, fig. 8) are provided on a bottom surface of said block body and are inserted into pin receiving holes formed in the stack of circuit boards (fig. 8), and the circuit boards in the stack are fixed to one another by fusing end portions of the anchor pings (another 72, fig. 8) extending from the other surface of the stack of circuit boards (fig. 8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the resin housing body to enclose the connecting pins as taught by Eck in the circuit boards of the electronic device of Rogers et al., in order to use the resin housing body to protect the connecting pins, and to tack plural electrical circuit boards in order to achieve a desired board packaging density and/or to enhance system speed (Eck, col. 1, line 17).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US-7099155 US-5017145 US-6265842 US-4780957.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiaoliang Chen whose telephone number is (571)272-9079. The examiner can normally be reached on 8:00-5:00 (EST), Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jinhee Lee can be reached on 571-272-1977. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Xiaoliang Chen/
Examiner, Art Unit 2841

Xiaoliang Chen
Examiner
Art Unit 2841